REMARKS

Claims 1-20 remain in the present application. Applicants respectfully request further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Claim Rejections – 35 U.S.C. §103

Claims 1-3, 6, 10-11 and 15-16

Claims 1-3, 6, 10-11 and 15-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent Number 5,994,937 to Hara et al. (hereafter referred to as "Hara"), in view of United States Patent Number 5,926,045 to Kwon (hereafter referred to as "Kwon"), and further in view of United States Patent Number 6,031,366 to Mitsuishi (hereafter referred to as "Mitsuishi"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 1-3, 6, 10-11 and 15-16 are not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1, which recites a timer circuit comprising (emphasis added):

> an output stage coupled to a configurable delay element; and
> a pull-down path coupled to said output stage and comprising a circuit for providing a selectable amount of pull down current, said pull-down path also coupled to receive a reference signal that varies in proportion to temperature and wherein a delay through said timer circuit is inversely proportional to said temperature.

Independent Claim 10 recites similar limitations to independent Claim 1. Claims 2-3 and 6 depend from independent Claim 1 and recite further limitations to the claimed invention. Claims 11 and 15-16 depend from independent Claim 10 and recite further limitations to the claimed invention.

Applicants respectfully submit that Hara fails to teach or suggest the limitation of a "configurable delay element" as recited in independent Claim 1. As recited in the present application, a timer circuit includes a configurable delay element.

In contrast to the claimed embodiments, Applicants understand the cited portion of Hara to teach a conventional inverter 402 as shown in Figure 4 (col. 3, lines 27-28). Applicants respectfully submit that Hara is silent with regard to inverter 402 being configurable as claimed. Although Hara may teach that inverter 404 is adjustable based upon a reference voltage (col. 3, lines 41-49), Applicants respectfully submit that an adjustable inverter is very different from a configurable delay element (e.g., configurable by a plurality of bits) as claimed. As such, Applicants respectfully submit that Hara fails to teach or suggest a configurable delay element as claimed.

Applicants respectfully submit that both Kwon and/or Mitsuishi, either alone or in combination with Hara, fail to cure the deficiencies of Hara discussed above with respect to independent Claim 1. Specifically, Applicants respectfully submit that Kwon and Mitsuishi also fail to teach or suggest the limitation of a "configurable delay element" as recited in independent Claim 1.

Furthermore, Applicants respectfully assert that no suggestion or motivation to combine Hara, Kwon and Mitsuishi in the claimed fashion has been shown sufficiently to establish a prima facie case of obviousness, as discussed in MPEP §2143. Applicants respectfully assert that Hara, Kwon and/or Mitsuishi, either explicitly or inherently, do not provide a motivation or suggestion to combine the references in the claimed fashion. Moreover, the references teach

away from such combination in the claimed fashion. For example, Hara teaches delay element 400 with N-FETs 414 and 424 for adjusting delay, while both Figure 2 of Kwon and Figure 3 of Mitsuishi teach variable current sources with a single node for coupling to other circuitry. As such, Applicants respectfully submit that combining either the variable current source of Kwon or Mitsuishi would render the delay element of Hara inoperable as it would necessitate removing N-FET 424 and leaving inverter 406 without a path to ground, and therefore, one of ordinary skill in the art would not be motivated to combine the references in the claimed fashion.

Furthermore, while N-FETs 414 and 424 in Figure 4 of Hara are tied to ground, the current source taught by Mitsuishi in Figure 3 is tied to power supply Vss. As such, Applicants respectfully submit that the references further teach away from one another for this reason, and therefore, one of ordinary skill in the art would not be motivated to combine the referenced in the claimed fashion.

For these reasons, Applicants respectfully submit that independent Claim 1 is not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since independent Claim 10 contains limitations similar to those discussed above with respect to independent Claim 1, independent Claim 10 also overcome the 35 U.S.C. §103(a) rejections of record. Since Claims 2-3, 6, 11 and 15-16 recite further limitations to the invention claimed in their respective independent Claims, Claims 2-3, 6, 11 and 15-16 also overcome the 35 U.S.C. §103(a) rejections of record. Thus, Claims 1-3, 6, 10-11 and 15-16 are therefore allowable.

Claims 4-5, 7-9, 12-14 and 17-20

Claims 4-5, 7-9, 12-14 and 17-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hara in view of Kwon, further in view of Mitsuishi, and further in view of United States Patent Number 6,388,490 to Saeki (hereafter referred to as "Saeki"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 4-5, 7-9, 12-14 and 17-20 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 17, which recites a method of varying a delay of a timer circuit comprising (emphasis added):

> during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;
> during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage; and
> during operation of said timer circuit, varying a reference signal coupled to said pull down path to vary delay though said timer circuit inversely proportional to temperature of said timer circuit.

Claims 18-20 depend from independent Claim 17 and recite further limitations to the claimed invention.

Applicants respectfully submit that Hara fails to teach or suggest the limitation of a "during configuration of said timer circuit, setting a first plurality of

configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit" as recited in independent Claim 17. As recited in the present application, a plurality of configuration bits are set during configuration of a timer circuit to adjust the delay through the timer circuit.

In contrast to the claimed embodiments, Applicants understand Hara to teach a delay circuit without configuration bits (Figure 4). As such, Applicants respectfully submit that Hara fails to teach or suggest that a plurality of configuration bits are set during configuration of a timer circuit to adjust the delay through the timer circuit as claimed.

Applicants respectfully submit that Kwon, Mitsuishi and/or Saeki, either alone or in combination with Hara, fail to cure the deficiencies of Hara discussed above with respect to independent Claim 17. Specifically, Applicants respectfully submit that Kwon, Mitsuishi and Saeki also fail to teach or suggest the limitation of a "during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit" as recited in independent Claim 17.

Additionally, Applicants respectfully submit that Saeki, either alone or in combination with Hara, Kwon and/or Mitsuishi, fail to cure the deficiencies of the cited Hara/Kwon/Mitsuishi combination discussed above with respect to independent Claims 1 and 10. Specifically, Applicants respectfully submit that Saeki also fails to teach or suggest the limitation of a "configurable delay element" as recited in independent Claims 1 and 10.

For these reasons, Applicants respectfully submit that independent Claim 17 is not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since Claims 4-5, 7-9, 12-14 and 18-20 recite further limitations to the invention claimed in their respective independent Claims, Claims 4-5, 7-9, 12-14 and 18-20 also overcome the 35 U.S.C. §103(a) rejections of record. Thus, Claims 4-5, 7-9, 12-14 and 17-20 are therefore allowable.

CONCLUSION

Applicants respectfully submit that Claims 1-20 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

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BMF

Bryan M. Failing
Registration No. 57,974

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060